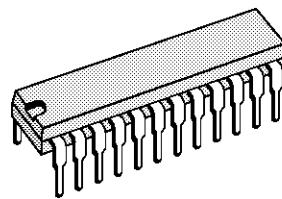


BUS-CONTROLLED AUDIO MATRIX

- 5 STEREO INPUTS
- 4 STEREO OUTPUTS
- GAIN CONTROL 0/2/4/6DB/MUTE FOR EACH OUTPUT
- CASCADABLE (2 DIFFERENT ADDRESSES)
- SERIAL BUS CONTROLLED
- VERY LOW NOISE
- VERY LOW DISTORSION



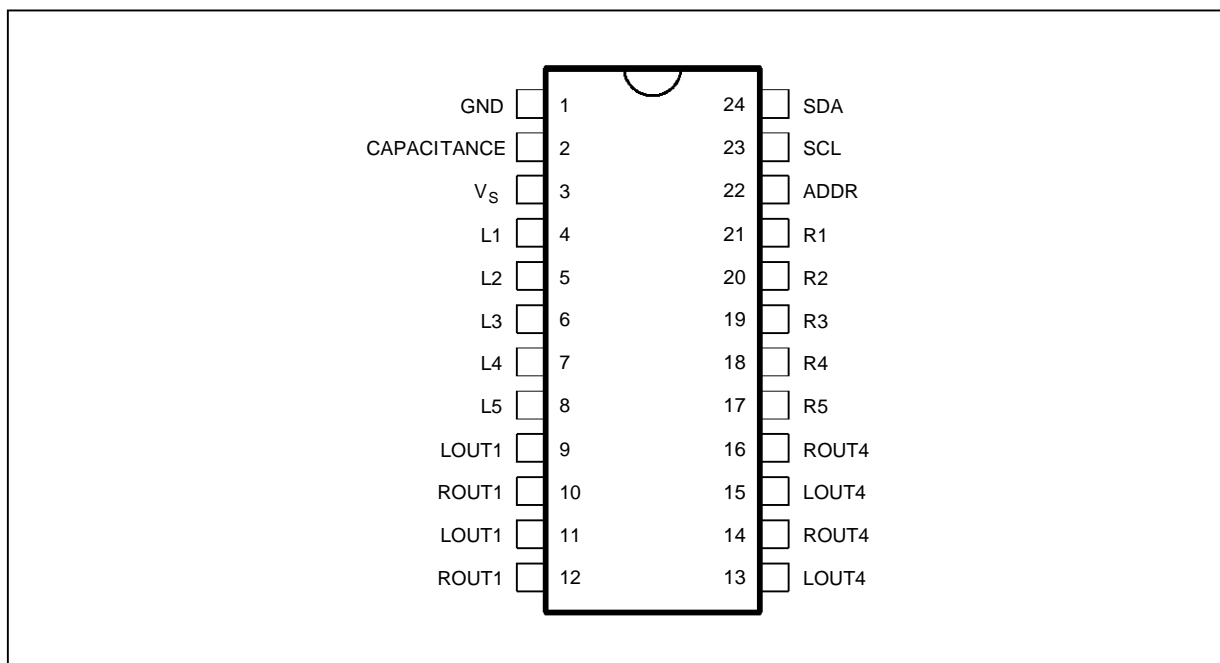
SHRINK 24
(plastic package)

ORDER CODE : TEA6420L

DESCRIPTION

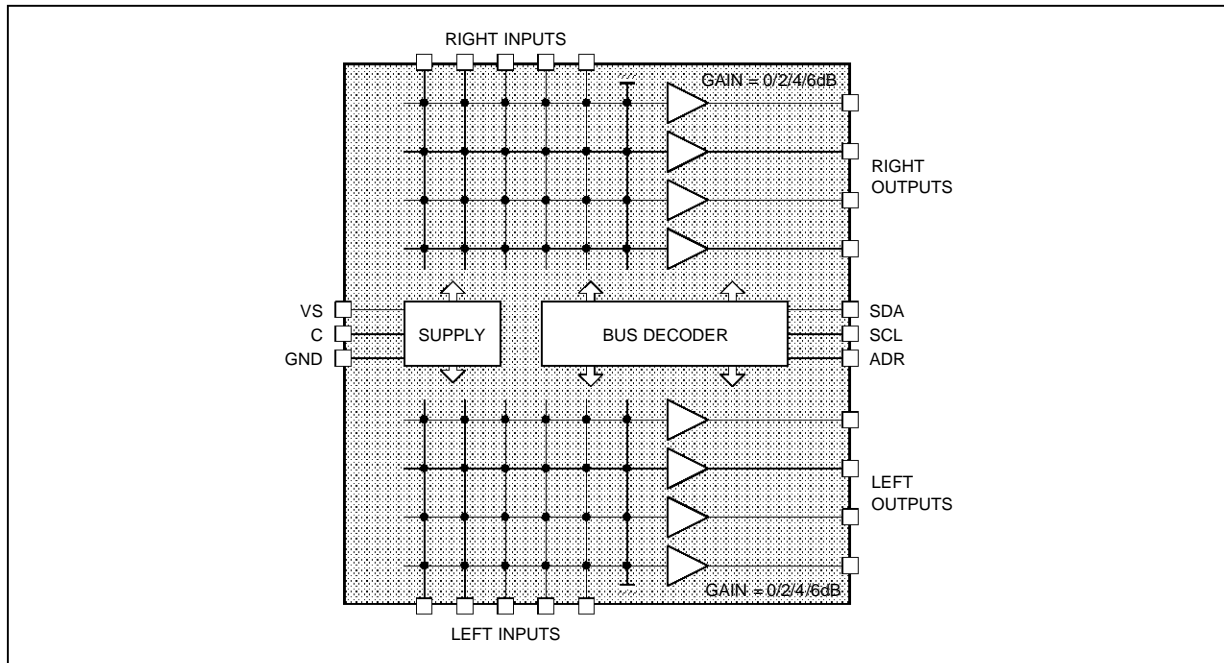
The TEA6420L switches 5 stereo audio on 4 stereo outputs.
All the switching possibilities are changed through the I²C BUS.

PIN CONNECTIONS



6420L-01.EPS

BLOCK DIAGRAM



6420L-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{cc}	Supply Voltage	10.2	V
T _{oper}	Operating ambient temperature	- 20 to + 85	°C
T _{stg.}	Storage Temperature	- 55 to + 150	°C

6420L-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th(j-a)}	Junction - ambient thermal resistance	75	°C/W

6420L-02.TBL

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 9V, R_L = 10kΩ, R_G = 600Ω, f = 1kHz (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

SUPPLY

V _S	Supply Voltage		8	9	10.2	V
I _S	Supply Current			5	8	mA
SVR	Ripple Rejection	W _{IN} = 500mV _{RMS} , BW = 20 - 20kHz		80		dB

MATRIX

V _{IN}	Input DC Level			5		V
R _I	Input Resistance		30	50		kΩ
C _S	Channel Separation	W _{IN} = 2V _{RMS} , BW = 20 - 20kHz		90		dB

OUTPUT BUFFER

V _{OUT}	Output DC Level			5		V
R _{OUT}	Output Resistance			50		Ω

6420L-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_S = 9\text{V}$, $R_L = 10\text{k}\Omega$, $R_G = 600\Omega$, $f = 1\text{kHz}$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

OUTPUT BUFFER (continued)

e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		μV
S/N	Signal to Noise Ratio	$V_{IN} = V_{OUT} = 1V_{RMS}$		110		dB
G_{min}	Min. Gain		-1	0	+ 1	dB
G_{max}	Max. Gain		5	6	7	dB
d	Distortion	$V_{IN} = V_{OUT} = 1V_{RMS}$		0.01		%
V_{CL}	Clipping Level	d = 0.3%	2	2.5		V_{RMS}
R_L	Output Load Resistance		2			$\text{k}\Omega$

BUS INPUT

V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage (pin 24)		4			V
I_I	Input Current		- 10		10	μA
V_O	Output Voltage	$I_O = 3\text{mA}$; SDA Acknowledge pin			0.4	V
R_{pu}	ADDR Pullup Resistor	Note		50		$\text{k}\Omega$

Note : R_{pu} is an internal pull-up resistor connected between the address programming pin ADDR and the internal positive supply voltage. Leaving ADDR disconnected or "floating" allows it to become logic 1. Connecting ADDR externally to the GND pin forces it to logic 0.

SOFTWARE SPECIFICATION**1. Chip address**

Address	HEX	ADDR
1010 1000	A8	0
1010 1010	AA	1

2. Data bytes

Output select								
X	0	0	G_1	G_0	I_2	I_1	I_0	Output 1
	0	1						Output 2
	1	0						Output 3
	1	1						Output 4
Input select								
X	Q_1	Q_0	G_1	G_0	0	0	0	Input 0
					0	0	1	Input 1
					0	1	0	Input 2
					0	1	1	Input 3
					1	0	0	Input 4
					1	0	1	Mute
Gain select								
X	Q_1	Q_0	0	0	I_2	I_1	I_0	Gain = 6 dB
			0	1				Gain = 4 dB
			1	0				Gain = 2 dB
			1	1				Gain = 0 dB

X = don't care

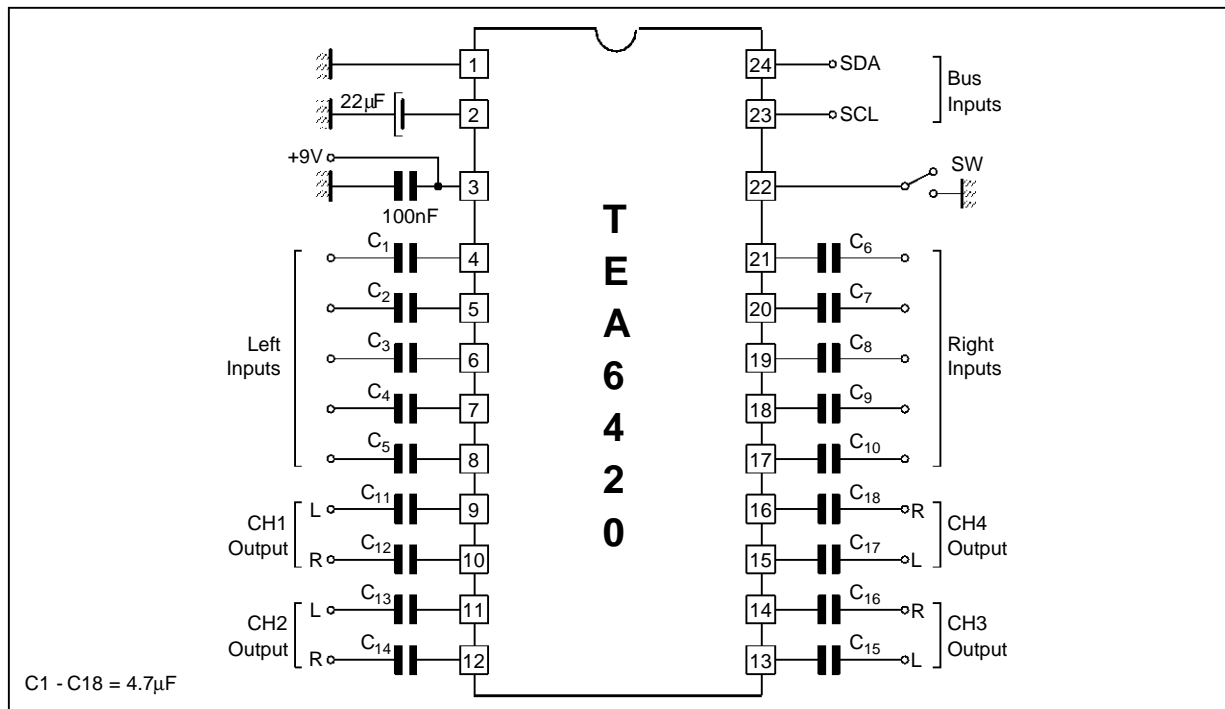
MSB is transmitted first

Example : 0 10 01 100 connects outputs 3 with input 4 at a gain of 4dB

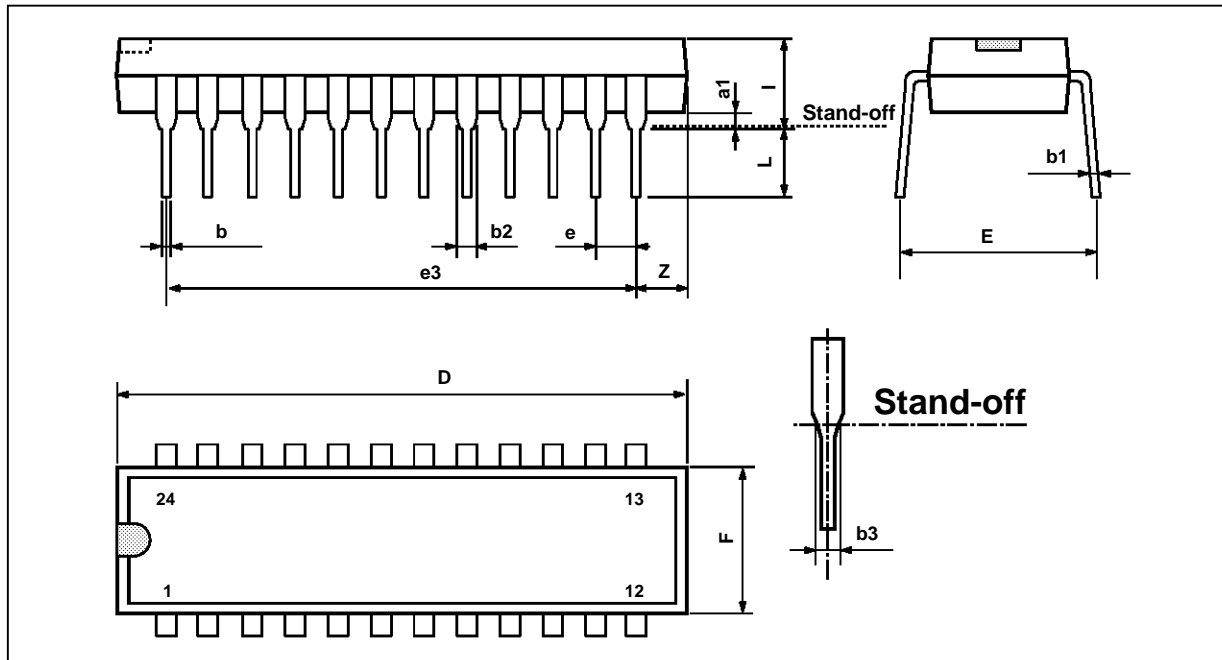
The following are selected after power-on reset : input 4 selected for all outputs ; gain = 0dB.

TEA6420L

TYPICAL APPLICATION



PACKAGE MECHANICAL DATA
24 PINS - PLASTIC SHRINK



PMSDIP24.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.51			0.020		
b	0.35		0.59	0.014		0.023
b1	0.2		0.36	0.008		0.014
b2	0.75		1.42	0.030		0.056
b3	0.75			0.030		
D			23.11			0.910
E	7.95		9.73	0.313		0.383
e		1.778			0.070	
e3		19.558			0.770	
e4		7.62			0.300	
F			6.86			0.270
i			5.08			0.200
L	2.54			0.100		

SDIP24.TBL

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